General Description

The HMC697LP4(E) wideband I/Q modulator is suitable to use with high-speed Digital to Analog converters (DAC) to transmit complex modulation schemes. In most of the applications, an interface circuit is required to ensure voltage compliance between the components, and low-pass reconstruction filtering to eliminate DAC output images.

Application Problem

In addition to the electrical compliance, proper DAC performance should be considered for RF transmit applications. The DAC sampling rate and resolution should be sufficient to represent the complexity of the transmitted signal. The maximum signal baseband bandwidth a DAC can output is limited by the Nyquist rate, which is defined as half the sampling rate. For example, a DAC with 800 Msps can generate baseband or IF signals up to the theoretical limit of 400 MHz. However, DAC output should be low-pass filtered to eliminate its images. Due to the finite roll off of this low pass filter the full bandwidth cannot be realized. After filtering, there should be sufficient bandwidth available for the transmitted signal. For this reason, especially for wideband and multi-carrier applications, high sampling rate DACs should be selected. Some DACs feature interpolation (oversampling) filters to reduce aliasing products and simplify external filtering requirements. Such components are recommended for the most demanding modulation schemes. In addition, the resolution of the DAC should be sufficient to represent complex modulation schemes with high crest factors. For direct conversion transmission applications, a DAC with built in complex digital modulation feature can be utilized. In this case, the HMC697LP4(E) will have sufficient IF bandwidth to directly convert IF to RF reducing the number of components in the transmit chain. Table 1 provides recommendations for minimum DAC performance requirements for most common RF transmit applications.

Table 1: Recommended minimum DAC performance requirements for selected RF transmit applications

	DAC Performance	
Application	Sampling Rate (Msps)	Resolution (# of bits)
GPRS	40	10
WLAN, WLL	125	10
GSM, W-CDMA, CDMA2000, IS-95, IS-136, EDGE (UWC-136)	250	10
Multicarrier GSM, WiMAX	500	12
LTE	1000	12

Application Solution

The remainder of this application note presents passive DC and AC coupled interface options between the HMC697LP4(E) and the most common off-the-shelf high-speed DACs, which have ±1V output compliance range. For support with other types of off-the-shelf DAC components, please contact Hittite Microwave customer support.

The selection of the DC or AC coupled connection depends on the application. The DC coupled solutions are advantageous for zero IF applications. However, they attenuate the baseband signal. On the other hand, AC coupled solutions do not attenuate AC signal, but block the near DC signal frequencies.

The following sections provide details of these interconnection options.

DC Coupled Interface with ±1V Compliance Range D/A Converters

The DC-coupled interface between the HMC697LP4(E) and an off-the-shelf DAC with ±1V output compliance range is presented in Figure 1. The connection is identical for I and Q ports.

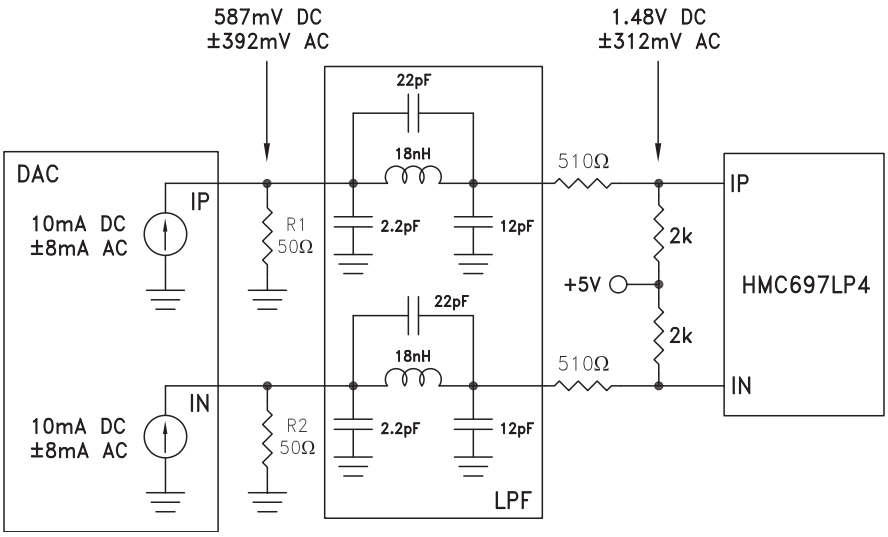

Figure 1. DC-coupled interface with ±1V DAC output compliance range

Routing and component mismatches should be minimized in order to prevent additional carrier leakage and unwanted sideband signals. Unless there is provision for calibration in the design, it is recommended to use 0.1% or better precision components for the interface circuits. The resistive interface network forms a voltage divider, and attenuates baseband input signal by 2 dB.

The low-pass DAC reconstruction filter should be designed specific to the application to eliminate DAC images. The input and output impedances of the filter can be optimized by splitting the R1 and R2 resistors on either side of the filter network. In this application, a 3rd order elliptic low-pass filter with 330 MHz 3 dB corner frequency is implemented as shown in Figure 1.

The HMC697LP4(E) has excellent uncalibrated carrier feedthrough (better than -40 dBm) and sideband suppression (better than -40 dBc) performance. However, calibration techniques can be implemented if further reduction in carrier feedthrough and unwanted sideband signal is required. The carrier feedthrough is reduced by compensating DC offset mismatches of the modulator I/Q channels. The sideband suppression is improved by compensating I/Q amplitude and phase mismatches. Many I/Q DACs have digital settings to adjust output DC offset voltage, amplitude, and phase to reduce carrier feedthrough and improve sideband suppression.

As an example, the HMC697LP4(E) is interfaced with an off-the-shelf DAC using the topology presented in Figure 1. The DAC is set for 10 mA DC current. The AC current swing is set to ±8 mA with 1.94 dB back-off from the full-scale current of ±10 mA. The circuit in Figure 1 results in 587 mV DC, ±392 mV AC voltage at the DAC output, and 1.48V DC, ±312mV single-ended AC (1.25V differential peak-to-peak) voltage at the modulator inputs. The resistive interface network attenuates the baseband AC voltage by ~2 dB.

Figure 2 Figure 3, and Figure 4 present the calibrated carrier feedthrough with 200 kHz sinusodial baseband inputs for LO frequencies at 900 MHz, 1900 MHz, and 3000 MHz respectively. Figure 5, Figure 6 and Figure 7 present the calibrated sideband suppression for the same frequencies. The calibration is done at mid-band at 25 °C, the calibration resolution at the baseband inputs for this implementation is: 15 µV DC offset, 0.067 dB I/Q amplitude balance, and 0.027° of I/Q phase offset.

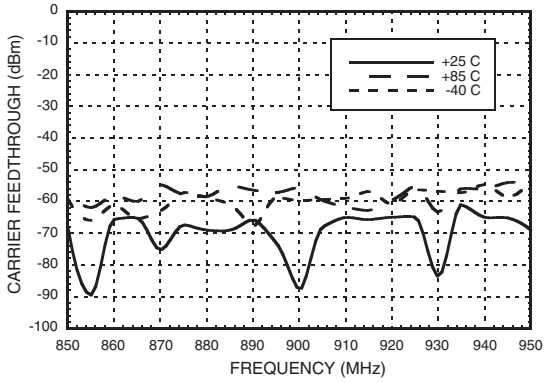

Figure 2. Calibrated carrier feedthrough for DC coupled interface @ LO = 900 MHz [1]

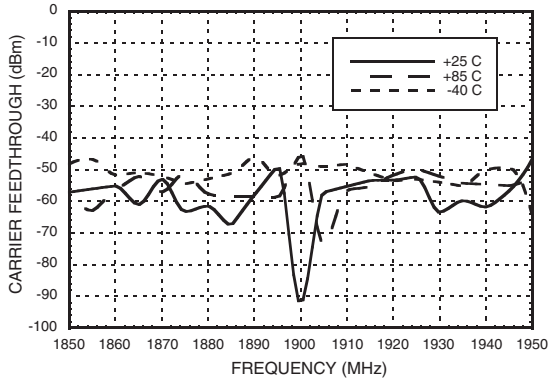

Figure 3. Calibrated carrier feedthrough for DC coupled interface @ LO = 1900 MHz [1]

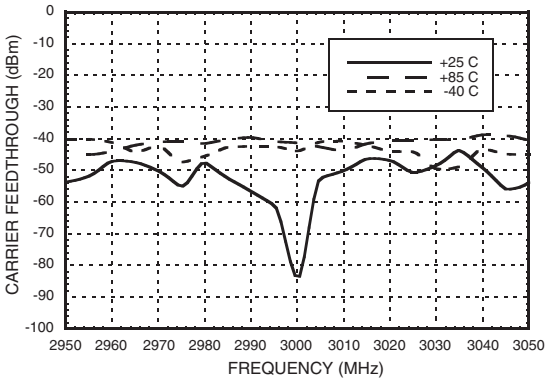

Figure 4. Calibrated carrier feedthrough for DC coupled interface @ LO = 3000 MHz [1]

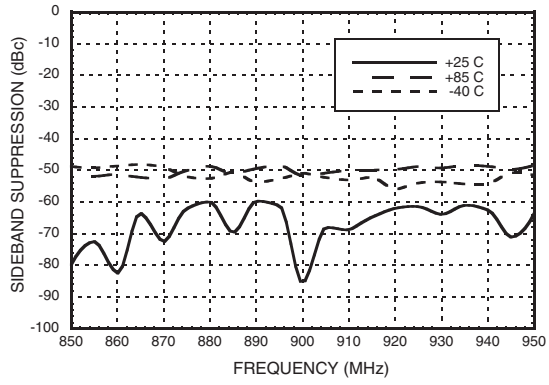

Figure 5. Calibrated sideband suppression for DC coupled interface @ LO = 900 MHz [1]

[1] Calibrated at 25 C, LO power = 0 dBm, baseband input frequency = 200 kHz

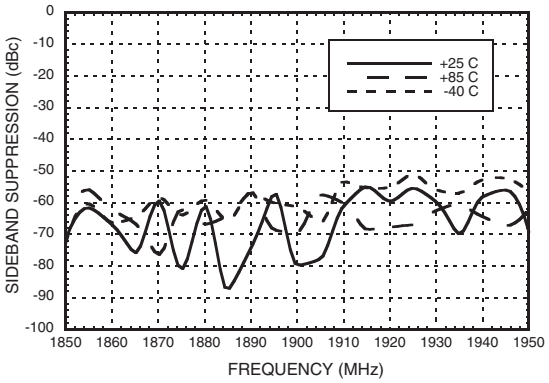

Figure 6. Calibrated sideband suppression for DC coupled interface @ LO = 1900 MHz [1]

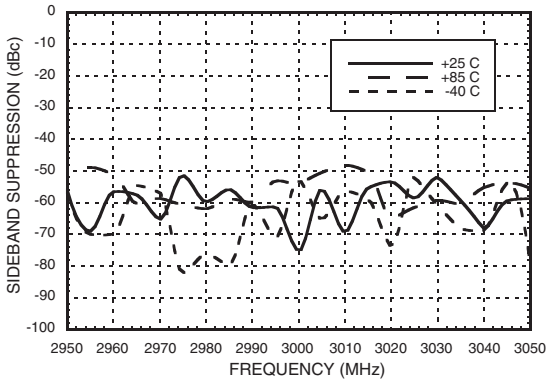

Figure 7. Calibrated sideband suppression for DC coupled interface @ LO = 3000 MHz [1]

AC Coupled Interface with ±1V Compliance Range D/A Converters

The DC coupled DAC-modulator interfaces have the advantage of utilizing digital DC offset cancellation features of DACs. However, the passive DC level shifting network attenuates the baseband signal. The AC coupled interface options eliminate this attenuation. Figure 8 shows the AC-coupled interface between the HMC697LP4(E) and a DAC with ±1V output compliance range. The DAC current output range is 0-20mA, and the connection is identical for I and Q ports.

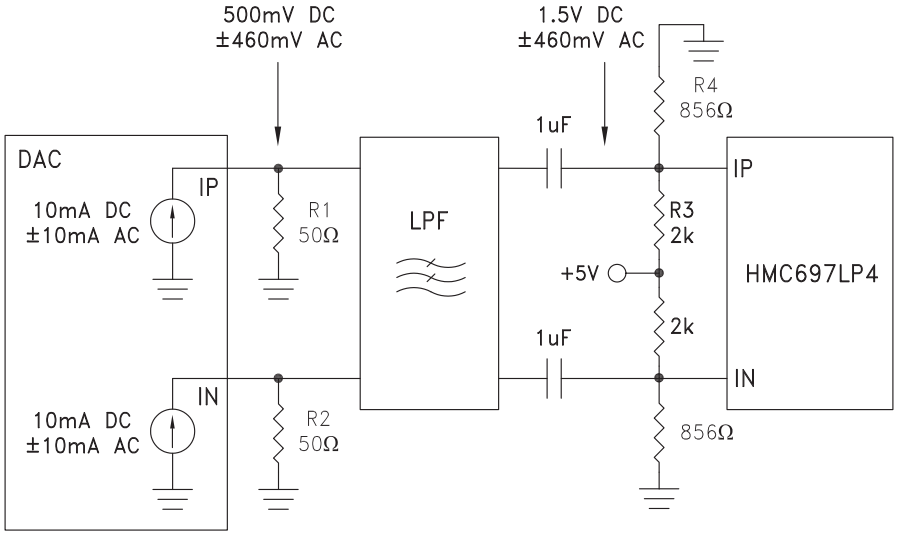

Figure 8. AC-coupled interface with ±1V DAC output compliance range

The DC block capacitor isolates the DC voltage domains of the DAC and the modulator. It is important to note that DC block capacitor presents a high pass filter effect, which should be considered for very low baseband frequencies. For this reason a large DC block capacitor value is chosen (1µF) to create a high pass corner of 245 Hz.

[1] Calibrated at 25 C, LO power = 0 dBm, baseband input frequency = 200 kHz

Routing and component mismatches should be minimized in order to prevent additional carrier leakage and unwanted sideband signals. Unless there is provision for calibration in the design, it is recommended to use 0.1% or better precision components for the interface circuits.

The low-pass DAC reconstruction filter should be designed specific to the application to eliminate DAC images. The input and output impedances of the filter can be optimized by splitting the R1 and R2 resistors on either side of the filter network.

Depending on the application, digital calibration features of the DACs can be implemented. Many DACs have phase, and amplitude calibration features that improve sideband suppression. While the main DAC output DC offset adjustment features cannot be used in the AC coupled case, R3 or R4 resistors can be replaced with potentiometers to calibrate carrier feedthrough. As an alternative, separate DACs or auxiliary DAC outputs that provide small DC currents can be implemented for DC offset calibration.

As an example, HMC697LP4(E) is AC-coupled with an off-the-shelf DAC using the circuit in Figure 9. In order to calibrate sideband suppression, amplitude and phase adjustments are performed from the main DAC outputs. The carrier feedthrough is calibrated by the auxiliary (AUX) outputs, which provide small amount of current to tune differential DC offset levels of the I/Q inputs. The low-pass filter block in Figure 9 is the 3rd order elliptic filter shown in Figure 1.

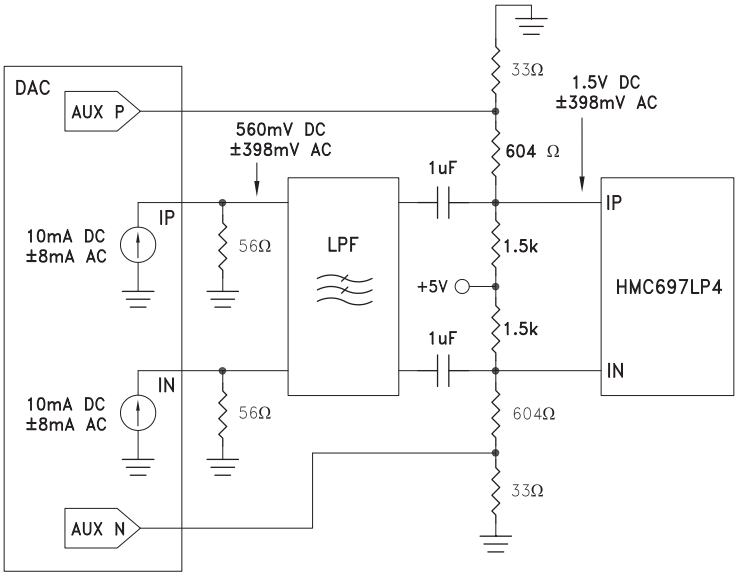

Figure 9. AC-coupled interface with main and auxiliary DAC outputs

The DAC is set for 10 mA DC current, and 1.94 dB back-off from the full-scale current (±8 mA AC). This results in 560 mV DC, ±398 mV AC swing at the DAC output, and 1.5V DC, ±398 mV single-ended AC (1.59V differential peak-to-peak) voltage at the modulator inputs.

Figure 10, Figure 11 and Figure 12 present the calibrated carrier feedthrough with 200 kHz sinusodial baseband inputs for LO frequencies at 900 MHz, 1900 MHz, and 3000 MHz respectively. Figure 13 Figure 14, and Figure 15 present the calibrated sideband suppression for the same frequencies. The calibration is done at mid-band at 25 °C. In this case, the calibration resolution is: 50 µV DC offset, 0.067 dB I/Q amplitude balance, and 0.027 degrees of I/Q phase offset.

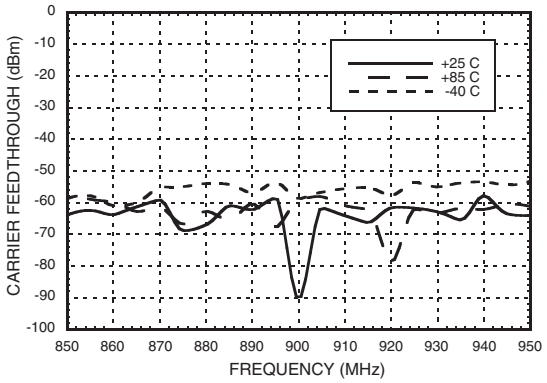

Figure 10. Calibrated carrier feedthrough for AC coupled interface @ LO = 900 MHz [1]

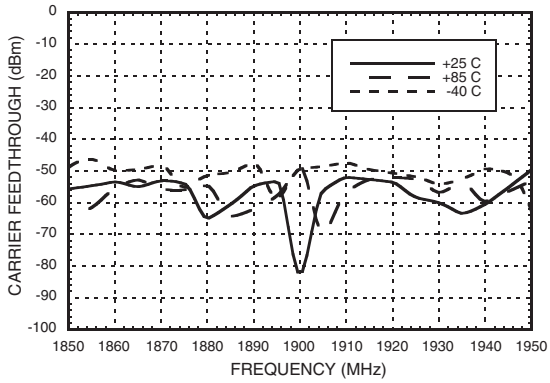

Figure 11. Calibrated carrier feedthrough for AC coupled interface @ LO = 1900 MHz [1]

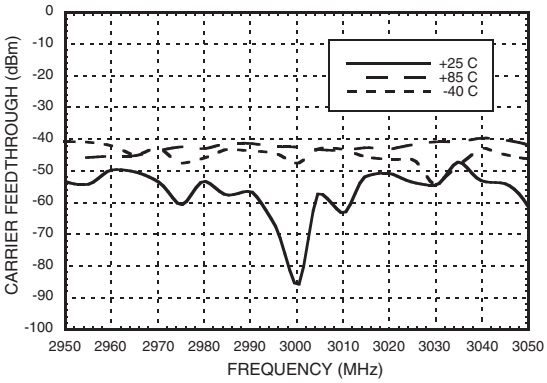

Figure 12. Calibrated carrier feedthrough for AC coupled interface @ LO = 3000 MHz [1]

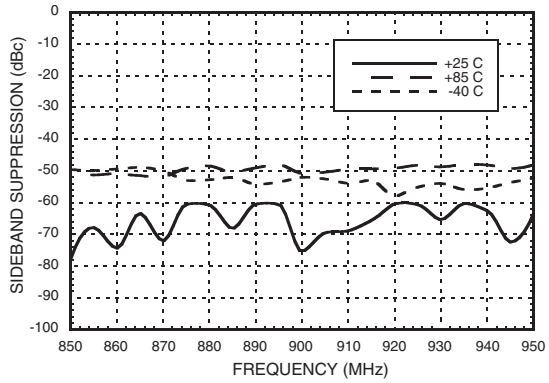

Figure 13. Calibrated sideband suppression for AC coupled interface @ LO = 900 MHz [1]

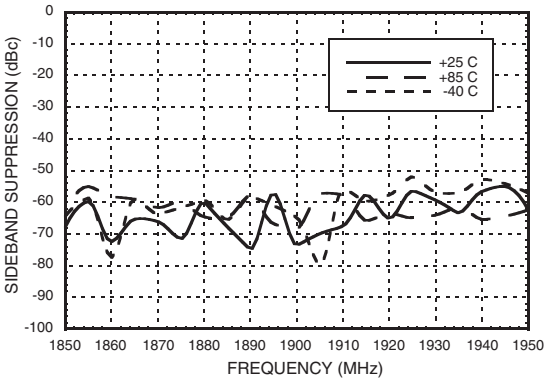

Figure 14. Calibrated sideband suppression for AC coupled interface @ LO = 1900 MHz [1]

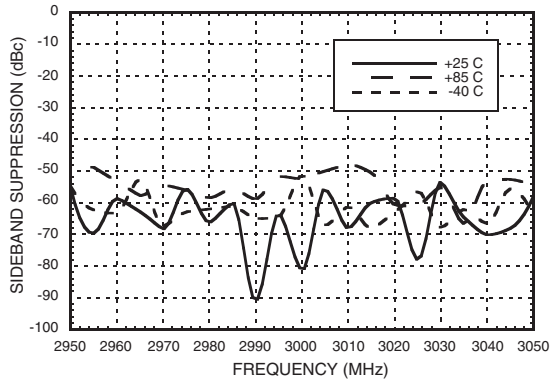

Figure 15. Calibrated sideband suppression for AC coupled interface @ LO = 3000 MHz [1]

[1] Calibrated at 25 C, LO power = 0 dBm, baseband input frequency = 200 kHz

Conclusion

The HMC697LP4(E) wideband I/Q modulator is suitable to use with high-speed Digital to Analog converters (DAC) to transmit complex modulation schemes. The transmitter DAC should be selected according to the complexity of the modulated signal in both time and amplitude. In this application note, the HMC697LP4(E) passive DC and AC interface options with most common off-the-shelf high-speed DAC's are presented. The calibrated sideband rejection and LO feedthrough of the HMC697LP4(E) are presented for various LO frequencies. Depending on the calibration resolution, the unwanted sideband and LO feedthrough can be reduced significantly.